

Fig. 1

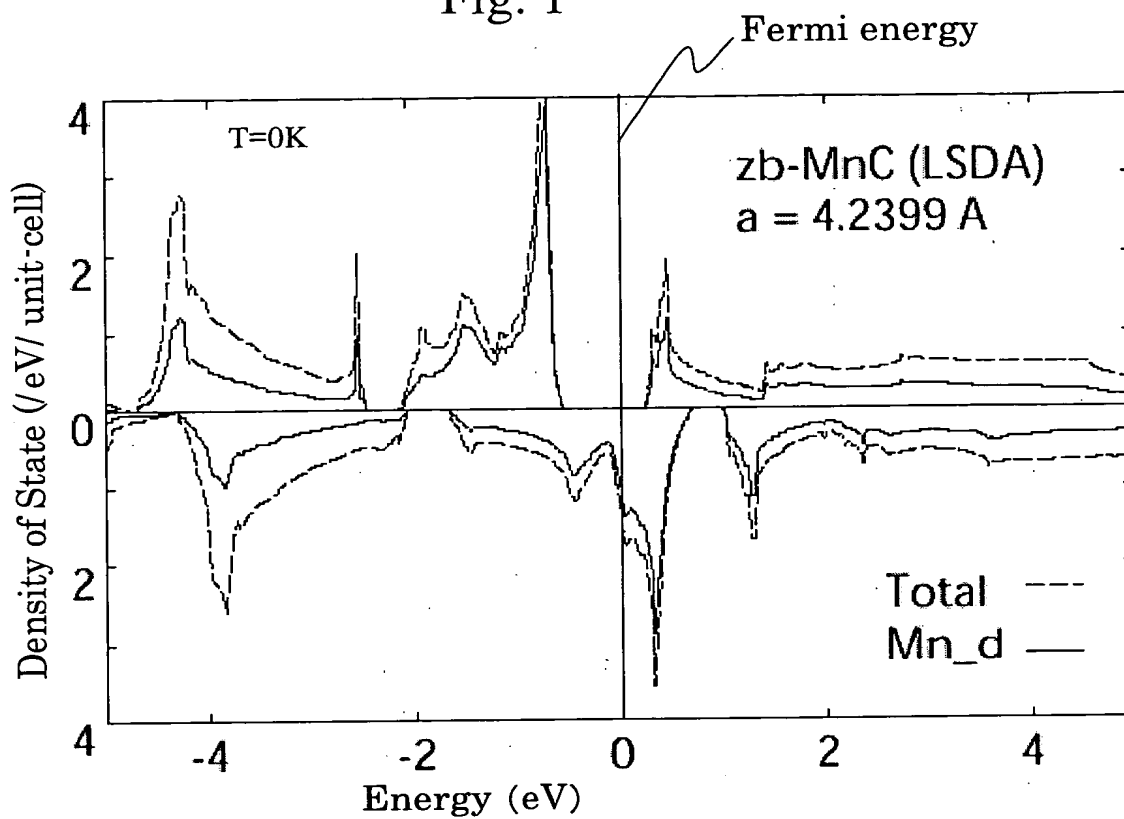


Fig. 2

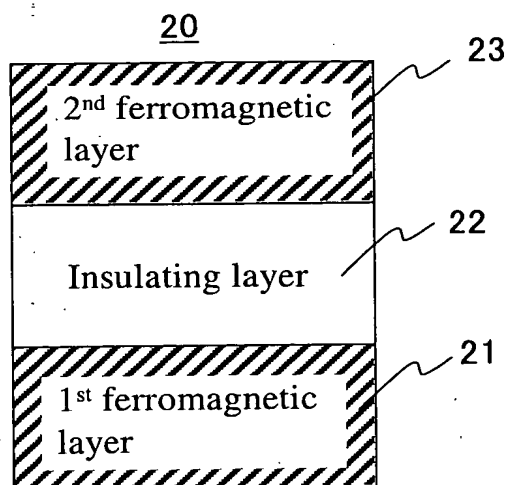


Fig. 3

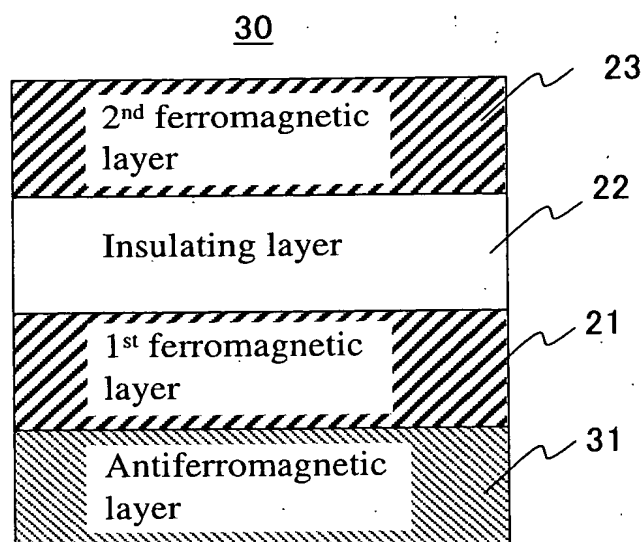


Fig. 4

40

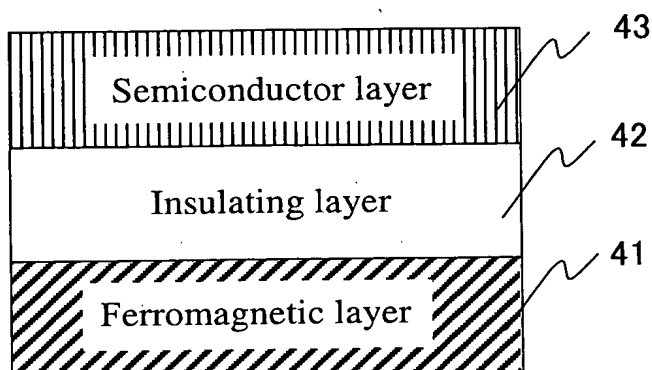


Fig. 5

50

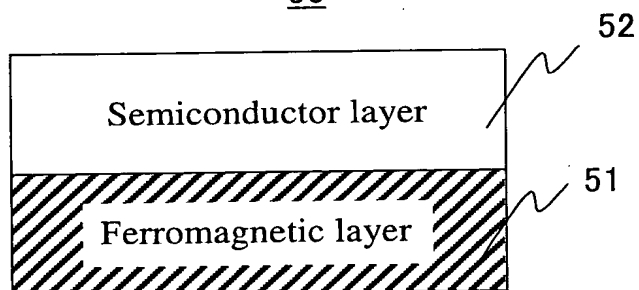


Fig. 6

60

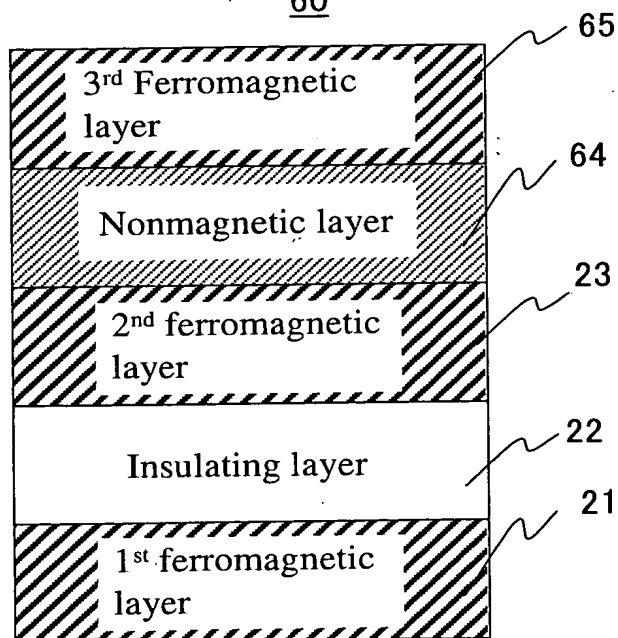


Fig. 7

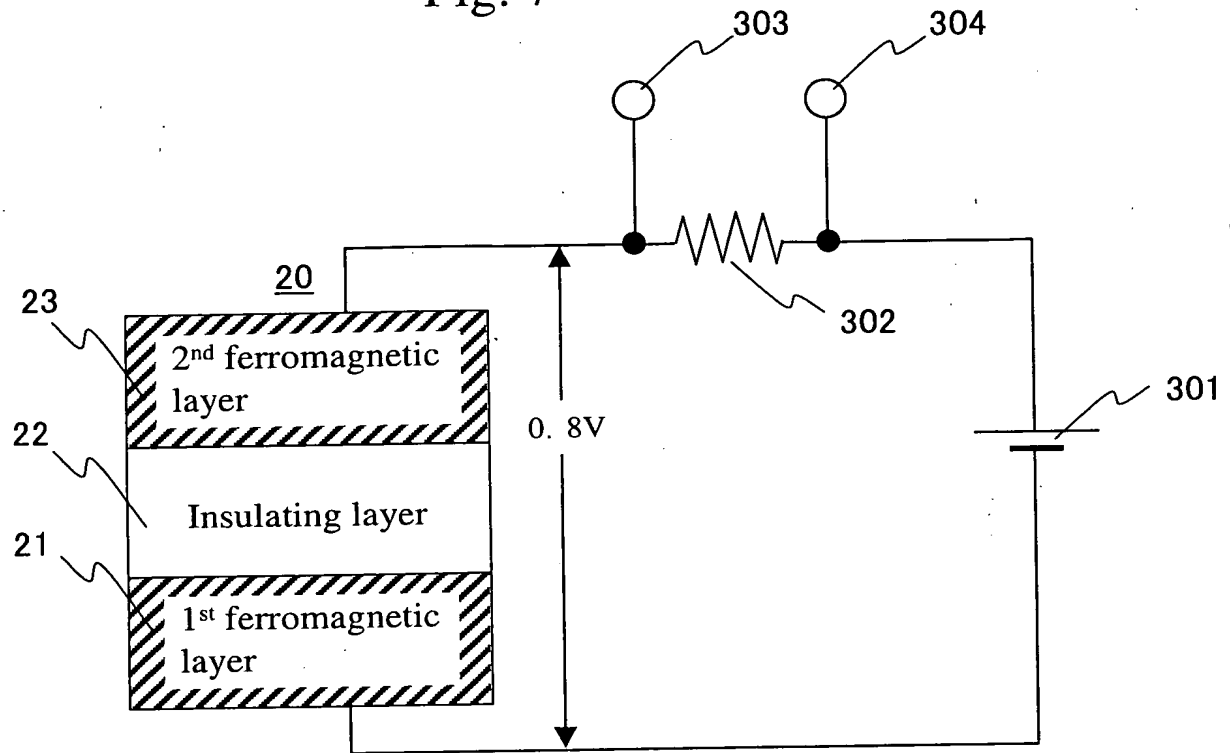


Fig. 8

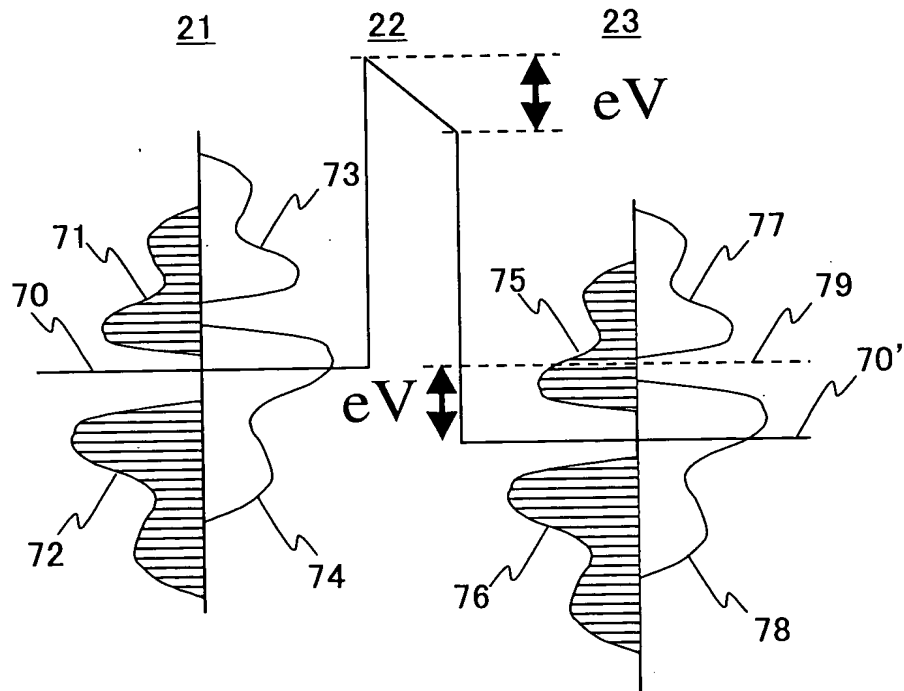


Fig. 9

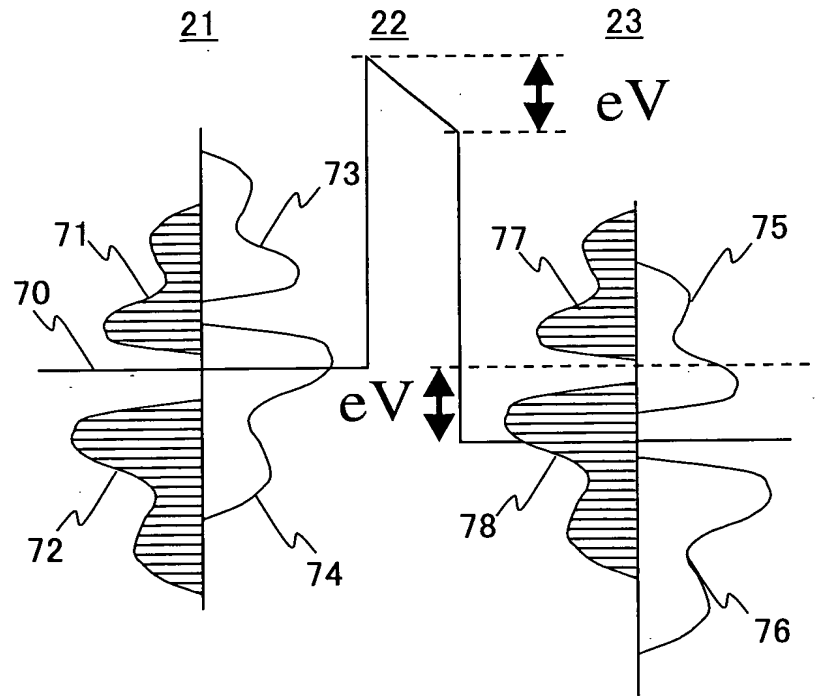


Fig. 10

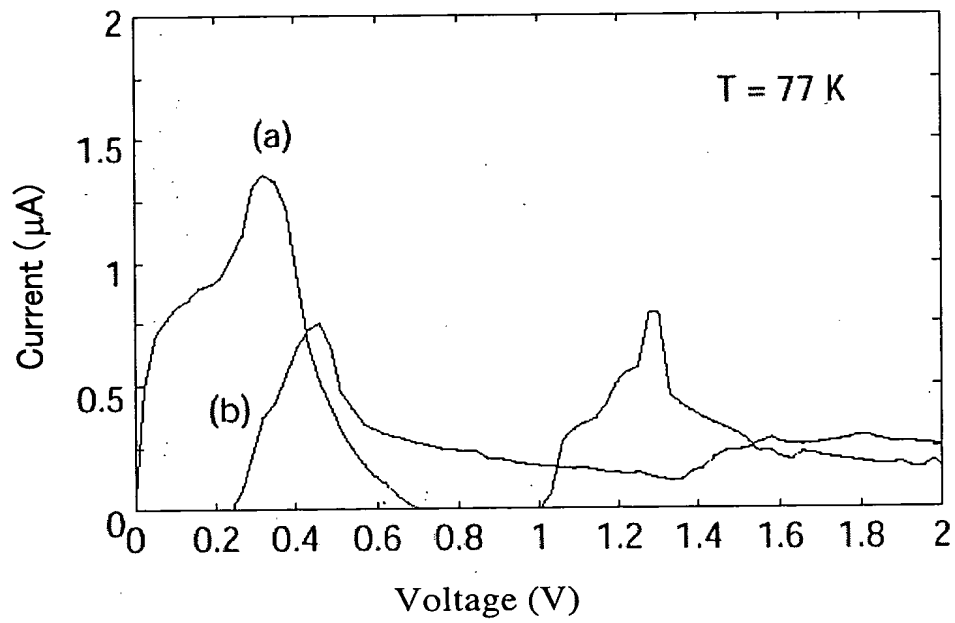


Fig. 11

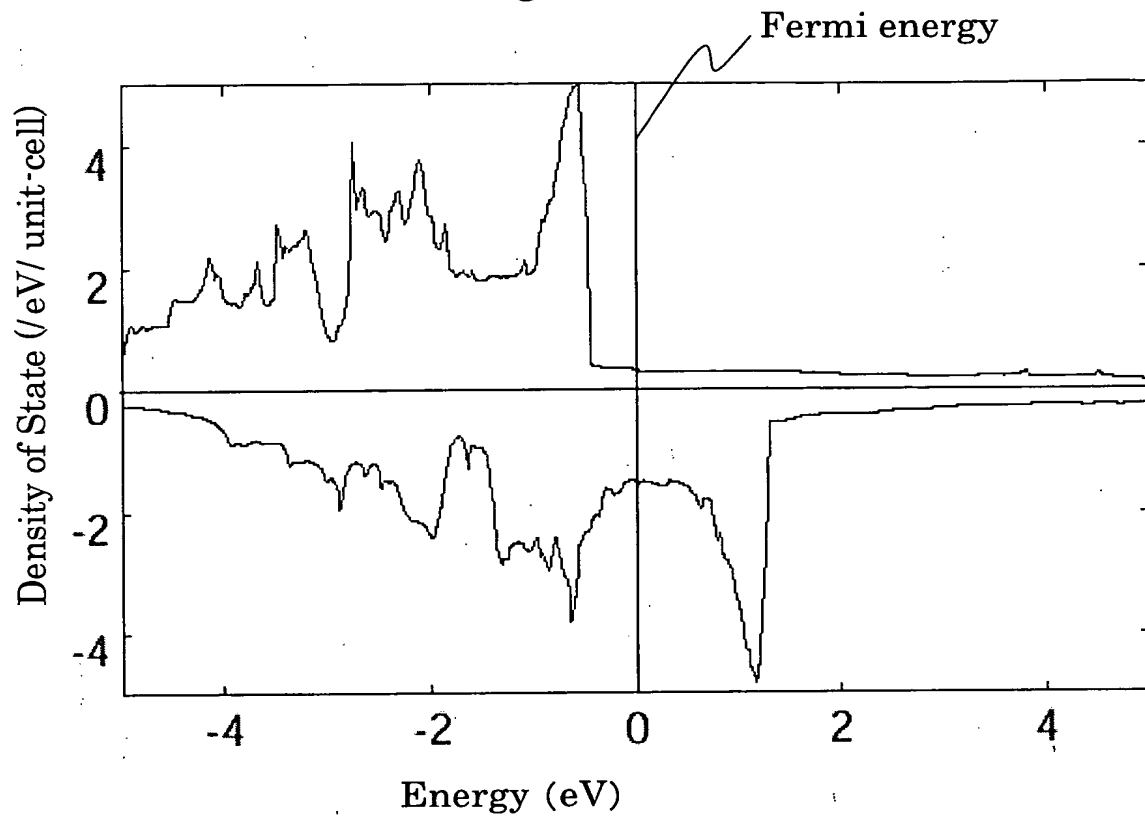


Fig. 12

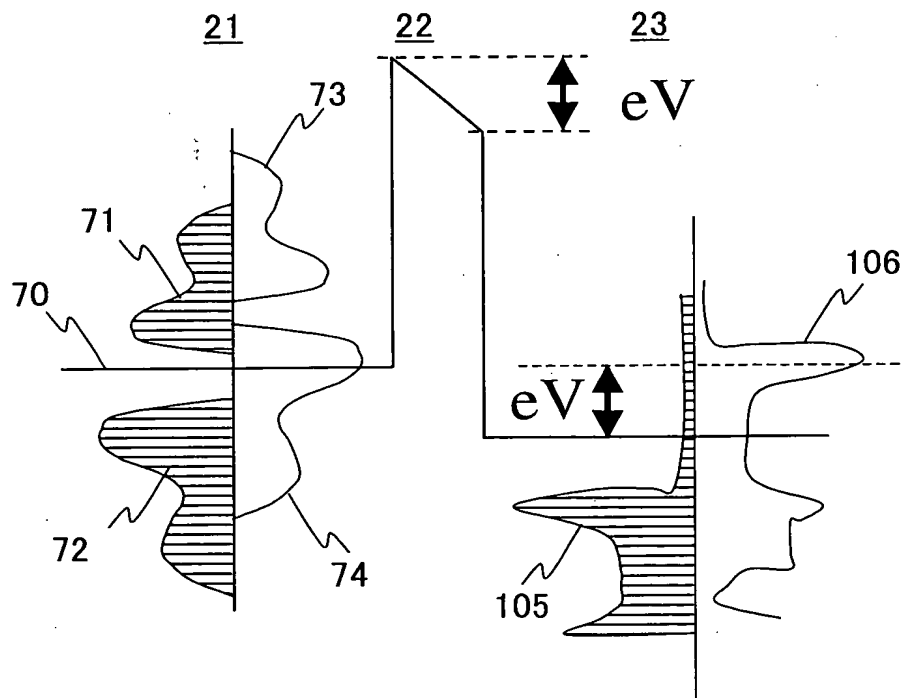


Fig. 13

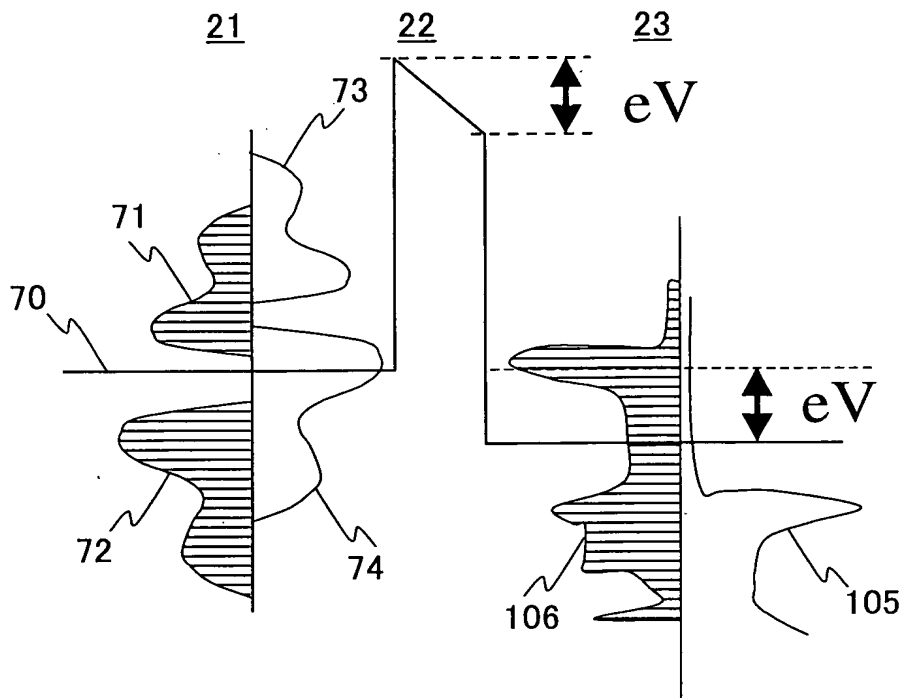


Fig. 14

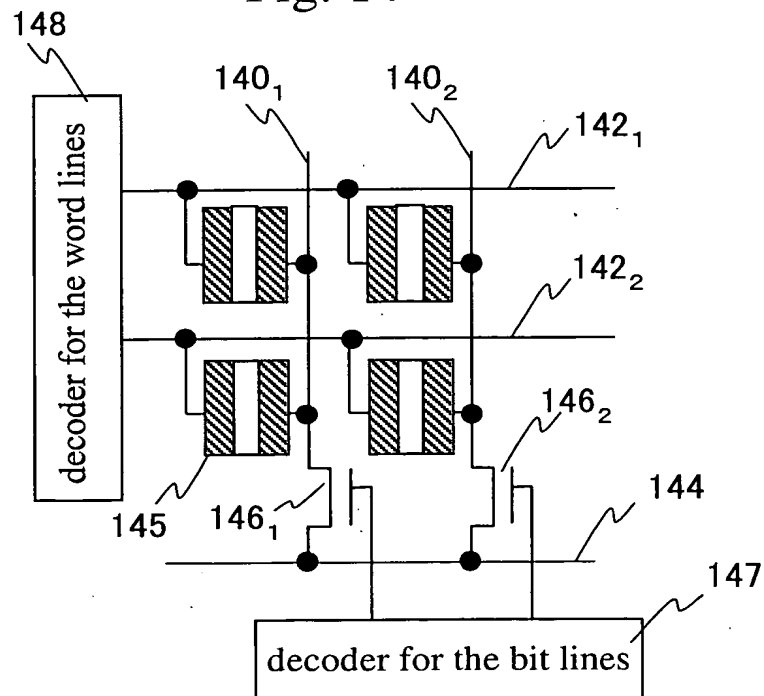


Fig. 15

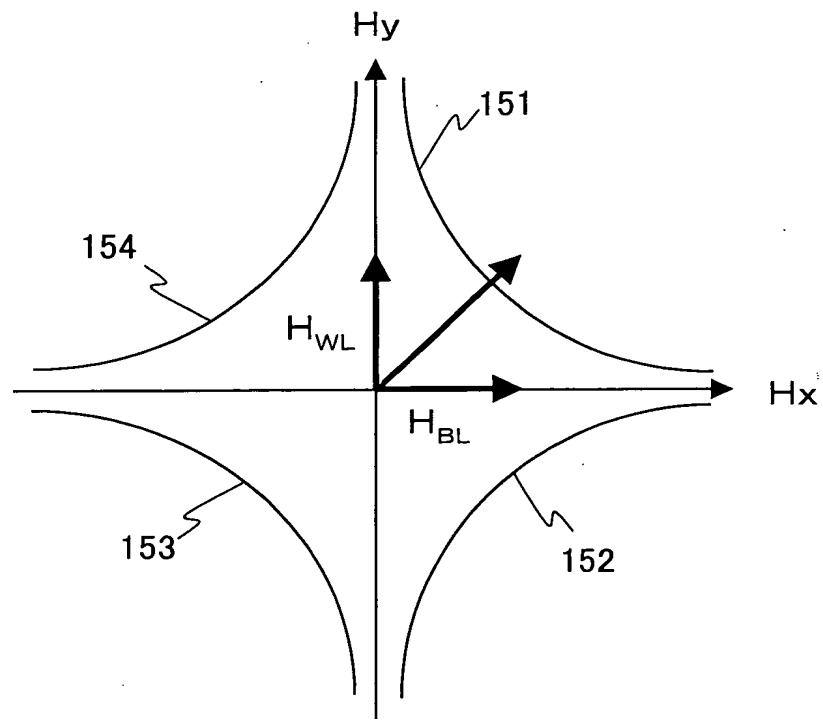


Fig. 16

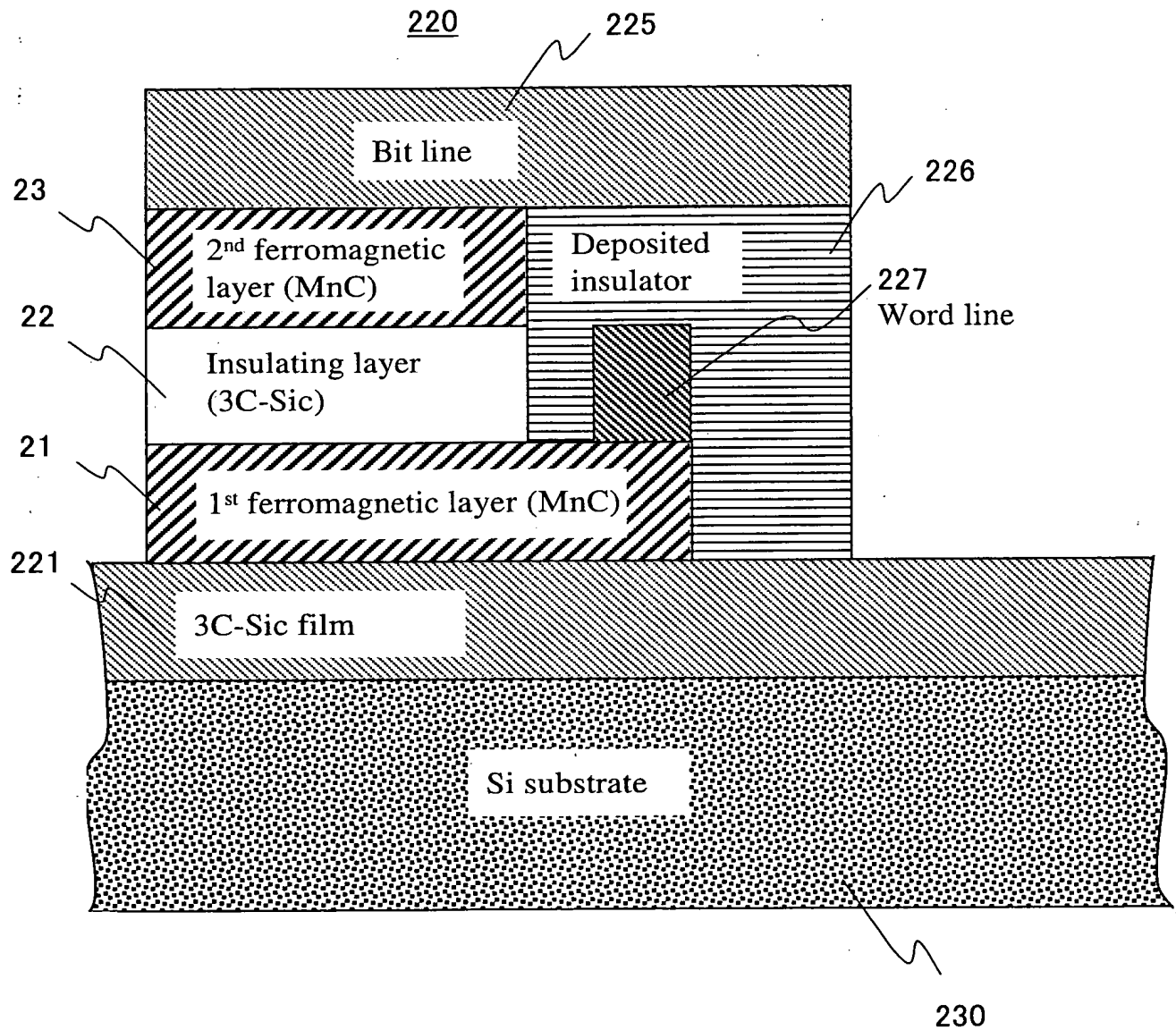
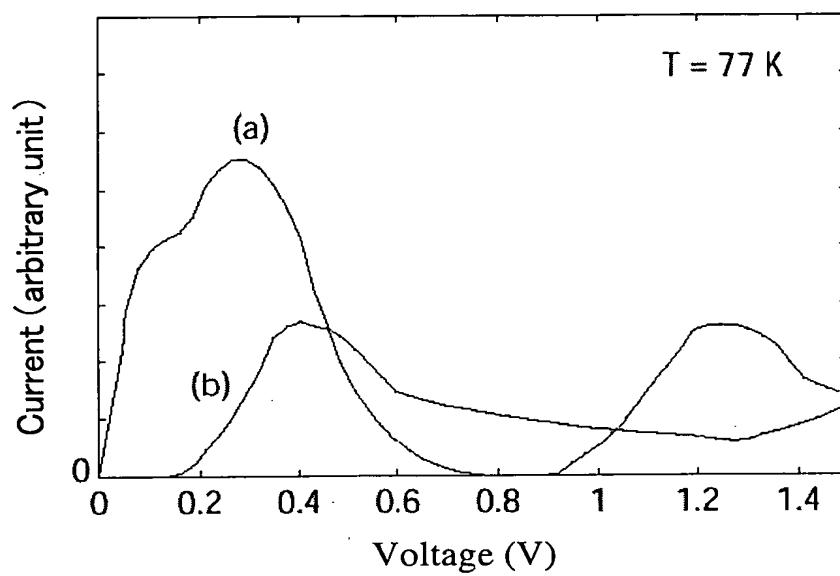


Fig. 17



The schematic diagram illustrates a memory array 144. It features a grid of word lines 142 (labeled 142₁ and 142₂) and bit lines 146 (labeled 146₁₁, 146₁₂, 146₂₁, and 146₂₂). A decoder for the word lines 148 is connected to the word lines. A decoder for the bit lines 147 (labeled 147₁ and 147₂) is connected to the bit lines. Access transistors 140 (labeled 140₁₁, 140₁₂, 140₂₁, and 140₂₂) are connected to the word lines and bit lines. Storage elements 146 (labeled 146₁₁, 146₁₂, 146₂₁, and 146₂₂) are connected to the bit lines. A reference voltage line 149 is also shown. The diagram includes various labels for components and lines, such as 148, 140₁₁, 140₁₂, 140₂₁, 140₂₂, 142₁, 142₂, 146₁₁, 146₁₂, 146₂₁, 146₂₂, 144, 149, 147₁, and 147₂.

Fig. 19

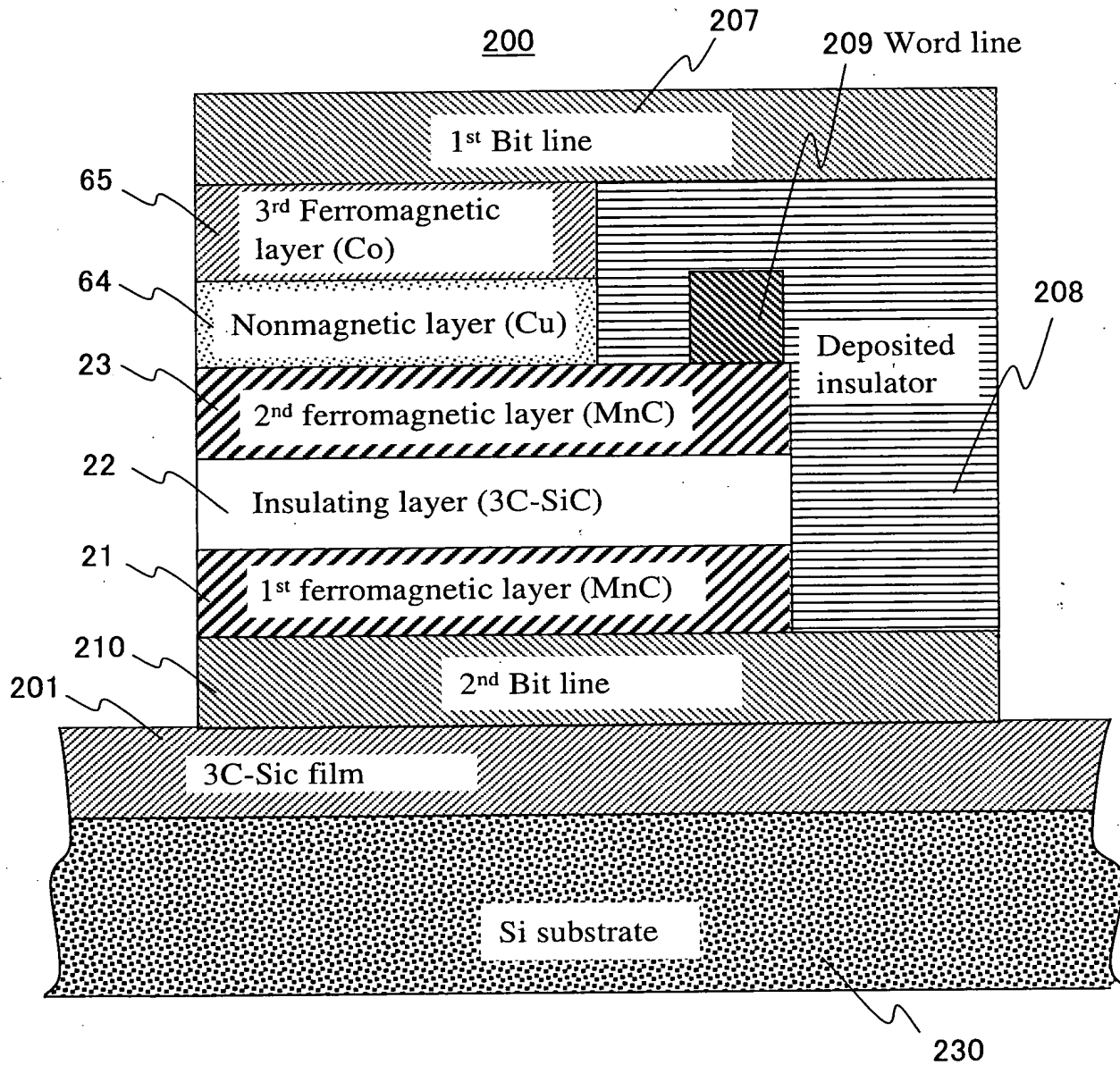


Fig. 20

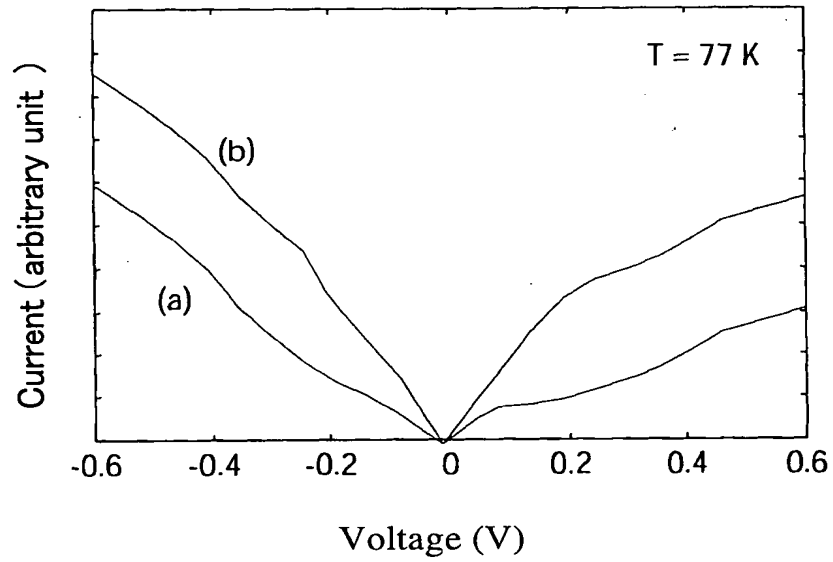


Fig. 21

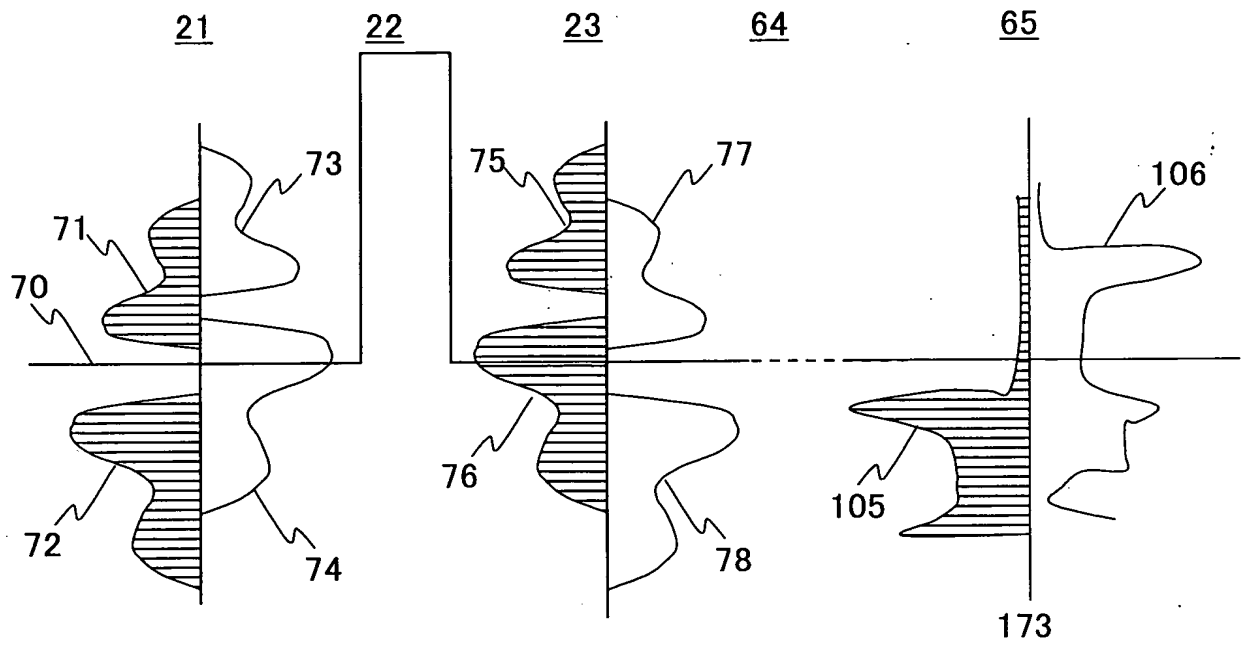


Fig. 22

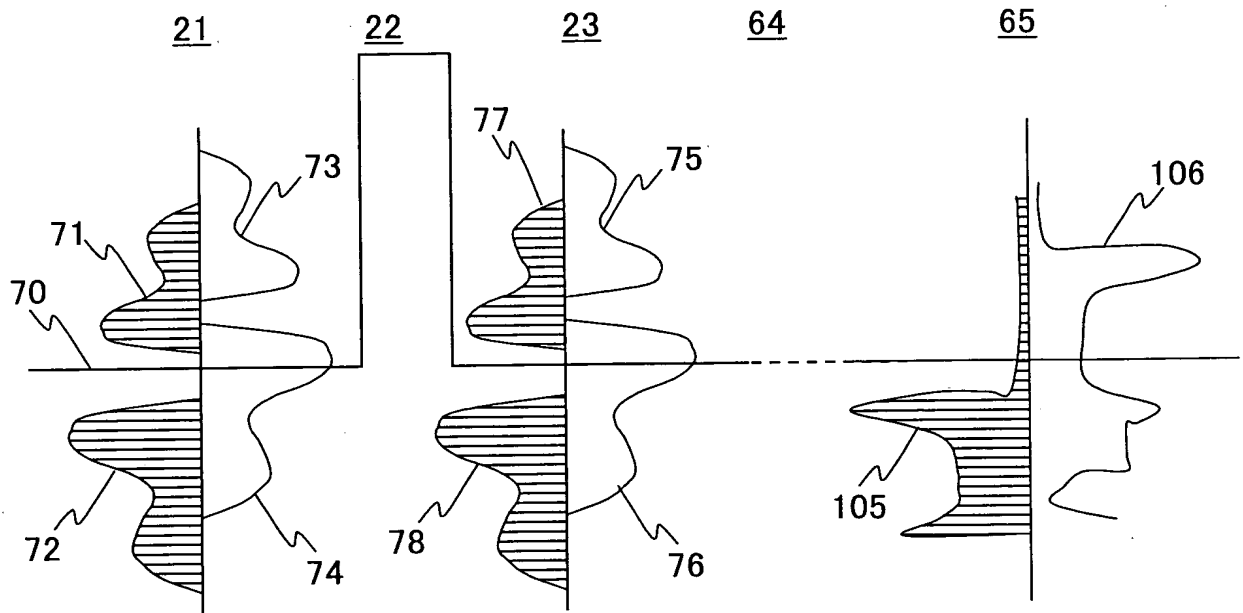


Fig. 23

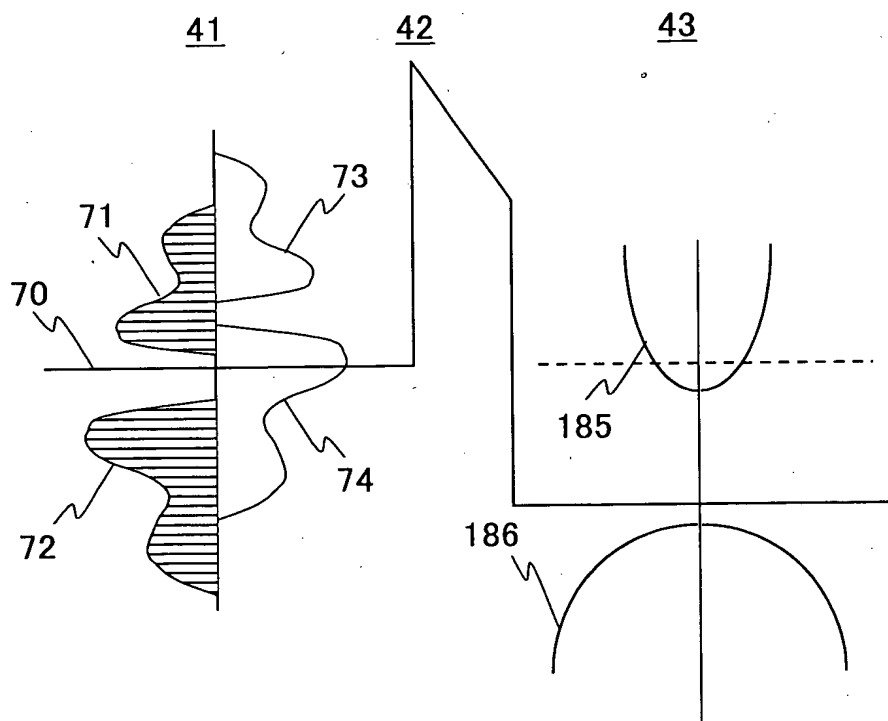


Fig. 24

